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BY

Bart Dierickx

Cornelis de Herdtstraat 8
B-2640 Mortsel
BELGIUM

FOR

A PIXEL STRUCTURE WITH IMPROVED CHARGE TRANSFER

A pix l structure with improved charg transfer

Background of the inv ntion

The present patent application is a continuation-in-part of patent application 09/460,630, the entire contents thereof being incorporated herein by reference.

Technical field of the invention

The present invention relates to pixel structures such as active or passive pixel sensors and pixel arrays for detecting electromagnetic radiation using, for example, MOS-based processing technology, e.g. CMOS technology. The pixel array may be used in a camera.

Description of related art

Commonly solid state image devices are implemented in a CCD-technology or in a CMOS or MOS technology.

CCD-technology is the name of a structure of adjacent MOS gates (usually NMOS devices; PMOS CCDs (Charge Coupled Devices) are not common but have been made) that allows both storage and transport of free charge. CCD imaging is performed in a three-step process: exposure of the CCD imaging device comprising an array of pixels, charge transfer, and charge-to-voltage conversion. By exposing the imaging device, an image is acquired when incident light in the form of photons falls on the array of pixels. The energy is absorbed in units called photons and a reaction takes place that creates an electron-hole pair. Exposure of the CCD imaging device thus converts light into an electronic charge at discrete sites called pixels. The charge transfer moves, at each clock pulse, the packets of charge within the silicon substrate towards an amplifier which is physically separated from the pixels. As the charge associated with one pixel moves, at the same time, the charges in all the pixels associated with that row or column move as well. For obtaining an accurate image, it is important that charges do not get lost during transfer. The packets of charge are eventually shifted to an output node, where electrons are converted to a voltage which is subsequently amplified. A disadvantage of CCD technology is that it cannot easily handle the other analog and digital functions that are critical on an imaging system level, such as analog to digital converters, precision amplifiers, memory, arithmetic units, and so on.

Of the image sensors implemented in a CMOS- or MOS-technology, image

sensors with passive pixels and image sensors with active pixels are distinguished. The difference between these two types of pixel structures is that a passive pixel does not perform signal amplification whereas an active pixel does. A passive pixel sensor is simply a photodiode (MOS or p-n junction diode) with a transistor that passes photoelectricaly generated signal charge to an amplifier outside the pixel array. The term "active pixel" refers to any pixel that has an active element, that is, at least one amplifier that typically comprises one or more transistors.

Passive pixel sensors usually make serious compromises in image quality. In this type of CMOS imager, a photosensitive diode or other junction converts photons into charge. Horizontal and vertical scan registers switch the charge that has been integrated in the pixels onto readout lines, much like in a conventional semiconductor memory, and subsequently amplify it. The primary difference between a CMOS imager and a memory circuit is the amplifier precision. Disadvantages of the simple passive-pixel CMOS imager architecture are a high noise level.

Active pixel sensors have a better noise performance than their passive pixel CMOS precursors, but typically suffer from a lower fill factor (= photosensitive portion of the pixel), and thus require a larger pixel size.

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However, the image quality of pixels with CMOS-technology is still less advanved than image quality of pixels with CCD-technology.

Due to the miniaturization of technology of CMOS based electronic circuits, it is possible to realize complex CMOS or MOS based pixels as small as CCD based pixels. It is a main advantage of CMOS or MOS based image sensors that CMOS technology is being offered by many foundries, whereas CCD technology is rarely offered and is a more complex and expensive technology option. Furthermore conventional CCD technology devices require significant power and a variety of input voltage levels (often in the 8-30 Volts range), while CMOS devices can be easily designed to draw only a small amount of current from a single low voltage power supply, which is important e.g. for hand-held devices.

Therefore there is an ongoing effort to increase the performance of CMOS or MOS image sensors such that a comparable image quality is obtained as the one obtained with high-end CCD images.

It is an object of the present invention to provide a pixel structure with improved charge transfer.

It is a further object of the present invention to obtain CCD-quality charge transfer using MOS-based technology.

It is yet a further object to provide an improved range pixel capable of operating at high speed.

It is also an object of the present invention to provide an array of pixels with improved properties, for instance, a synchronous shutter action.

Summary of the invention

The above objective is accomplished by providing a pixel structure comprising:

a semiconductor substrate;

a radiation sensitive source of carriers in the substrate;

a non-carrier storing, carrier collecting region in the substrate;

a doped or inverted region of a first conductivity type in or on the substrate; and

a non-carrier storing, planar current flow, carrier transport pathway from or through the carrier collecting region to the doped or inverted region. The pixel structure may be used in a camera. The carrier source is preferably non-carrier storing. In all the embodiments of the present invention the "carrier collecting region" may also be described as a carrier attracting region. In embodiments of the present invention the carrier transport pathway may be a separate transport region. Alternatively, it can be part of the carrier collecting region.

When the pixel structure is exposed to light, free carriers such as electrons are generated. These are not stored in the substrate. They are attracted or diffuse to the carrier collecting region, and are transferred by means of the transport pathway to the doped or inverted region, where they are collected for readout. By using non-carrier storing mechanisms and transport pathways the complete collected charge is transferred so that the quantitative amount of readout charge can be utilised. The readout circuitry connected to the doped or inverted region for reading out the pixel may be any suitable detection circuitry used in pixels (floating diffusion, etc).

The semiconductor substrate may be n-type or p-type silicon substrate; the doped or inverted regions may be p-type or n-type silicon. The pixel structure may be a passive or active pixel.

The pixel structure may further comprise at least one implant for confining the carrier collecting region. This implant or these implants may be provided for example at either side of the carrier collecting region.

The carrier collecting region may be a depletable region of the first conductivity type, i.e. with a concentration of dopant so low that it is in normal use always depleted. It may also be an, at least in part, pinned diode. In another

embodiment, the carrier collecting region may be silicon substrate under a covering layer of oxide. In still another embodiment, it may be silicon substrate covered by a field oxide layer. And in yet another embodiment, it may be silicon substrate covered by a polysilicon cover. The carrier transport pathway is preferably diffusion limited.

There is also provided, in accordance with the present invention, a range pixel of the type described above. The range pixel comprises:

a semiconductor substrate;

a radiation sensitive source of carriers in the substrate;

a non-carrier storing, carrier collecting region in the substrate;

at least two doped or inverted regions of a first conductivity type in or on the substrate; and

a non-carrier storing, planar current flow, carrier transport pathway from or through the carrier collecting region to each doped or inverted region. The range pixel may be an active or a passive pixel. It is preferably MOS-based. The range pixel may be used in a camera. The source is preferably non-carrier storing. In all the embodiments of the present invention the "carrier collecting region" may be described as a carrier attracting region. In embodiments of the present invention the carrier transport pathway may be a separate transport region. Alternatively, it can be part of the carrier collecting region.

Here again, the semiconductor substrate may be n-type or p-type silicon substrate; the doped or inverted regions may be p-type or n-type silicon. The carrier collecting regions may be depleted regions of a first conductivity type, i.e. with a concentration of dopant so low that it is in normal use always depleted. It may also be an, at least in part, pinned diode or buried diode. In another embodiment, the carrier collecting regions may be silicon substrate under a covering oxide layer, silicon substrate under a field oxide layer, or silicon substrate under a polysilicon cover layer. The carrier transport regions are preferably diffusion limited.

The present invention may provide a pixel array comprising at least one set of pixels of a first sensitivity and a second set of pixels of a second sensitivity, the first and second sensitivities being different from each other. The pixels may be active or passive pixels. The pixels are preferably MOS-based. The pixel array may be used in a camera.

The present invention may also provide a pixel array comprising a plurality of pixel structures, each pixel structure comprising:

a photosensitive element for converting radiation into charge carriers;

a carrier storing element;

a first switch located in-between said photosensitive element and said carrier storing element; and said photosensitive element also being connected to a voltage with a reset switch; and the pixel array further comprising:

a timing circuit for resetting all the pixels of the array simultaneously.

The present invention may also include a pixel array comprising a plurality of pixels, each pixel comprising:

a photosensitive element for converting radiation into charge carriers;

a carrier storing element;

a first switch located in-between said photosensitive element and said carrier storing element; and said photosensitive element also being connected to a voltage with a reset switch; and the pixel array further comprising:

a timing circuit for simultaneously opening the first switches of all the pixels of the array simultaneously.

The carrier storing element of at least one pixel in nay of the above arrays may be an analog memory element such as a capacitor or a parasitic capacitor. Each pixel may be MOS-based. An amplifier may be connected to each carrier storing element. The amplifier may be located within at least one pixel structure to have an active pixel. The amplifier may be placed outside at least one pixel structure to obtain a passive pixel. Any of the above pixel arrays may be used in a camera.

Other features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention.

Brief description of the drawings

Fig. 1 is a cross-sectional schematic representation of a first embodiment of an active pixel according to the present invention, with a non-carrier storing carrier collecting n-type region with a concentration of dopant so low that it is in normal use always depleted, a doped region and a non-carrier storing transport region.

Fig. 2 is a cross-sectional schematic representation of a second embodiment of an active pixel according to the present invention, used as a range pixel, and comprising a non-carrier storing carrier collecting n-type region with a concentration of dopant so low that it is in normal use always depleted, two doped regions and two non-carrier storing transport regions.

Fig. 3 is a cross-sectional schematic representation of a third embodiment of an active pixel according to the present invention, whereby the carrier collecting

region is a substrate under a covering oxide layer and two carrier non-storing transport pathways.

Fig. 4 is a schematic representation of a potential diagram for explanationof embodiments of the present invention.

Fig. 5 is a schematic representation of an array of elongated pixels.

Fig. 6a and Fig. 6b are, respectively, a schematic representation of a cross-section along a long axis of a first embodiment of an elongated pixel according to the present invention and a transverse cross-section thereof.

Fig. 6a and Fig. 6b are a schematic representation of a cross-section along a longitudinal axis of a first embodiment of an elongated pixel according to the present invention, respectively a transverse cross-section thereof, whereby the carrier collecting region comprises an n-type region with a concentration of dopant so low that it is in normal use always depleted.

Fig. 7a and Fig. 7b are schematic representations of a cross-section along a longitudinal axis of a second embodiment of an elongated pixel according to the present invention, respectively a transverse cross-section thereof, whereby the carrier collecting region is a substrate under a covering oxide layer.

Fig. 8a and Fig. 8b are schematic representations of a cross-section along a longitudinal axis of a third embodiment of an elongated pixel according to the present invention, respectively a transverse cross-section thereof, whereby the carrier collecting region is substrate under a field oxide layer.

Fig. 9a and Fig. 9b are schematic representations, respectively, of a cross-section along a longitudinal axis of a fourth embodiment of an elongated pixel according to the present invention, and a transverse cross-section thereof, whereby the carrier collecting region is a pinned diode.

Fig. 10a and Fig. 10b are schematic representations of a cross-section along a longitudinal axis of a fifth embodiment of an elongated pixel according to the present invention, and a transverse cross-section thereof, whereby the carrier collecting region is substrate under a polysilicon layer.

Fig. 11 is a cross-sectional schematic representation of a CCD made based on the structure represented in Fig. 10.

Fig. 12 represents an array of pixels of varying sensitivity.

Fig. 13a and Fig. 13b are symbolic representations of a synchronous shutter.

Fig. 14 is a cross-sectional schematic representation of a synchronous shutter according to an embodiment of the present invention.

Fig. 15a is a time diagram showing pulses occurring synchronously for all

pixels and lines of a synchronous shutter of Fig. 14 for integrating the generated charges. Fig. 15b is a time diagram showing pulses occurring for reading out line per line a synchronous shutter according to an embodiment of the present invention.

Description of the preferred embodiments

Persons skilled in the art will recognise that, in what follows, each part with as conductivity type either n-type or p-type can as well have as conductivity type respectively p-type or n-type, and that there are many values of the concentration densities which are compatible with the present invention. The word "carrier" may represent either "holes" or "electrons". The carrier collecting region 3 and the doped or inverted region 4 are formed using techniques well understood in the art, such as diffusion and implantation. Similarly, the electrode 7 and the insulation layer 2 are formed in conventional manners.

Fig. 1 illustrates a first embodiment of a pixel structure of the present invention formed in a semiconductor substrate 1 with dopant of a first conductivity type at a first concentration density. The pixel structure may be used in an active or passive pixel. In the preferred embodiment of Fig. 1, the semiconductor substrate 1 is a p-type silicon substrate. The concentration density of dopant in the substrate is typically between 1×10^{15} and $1 \times 10^{16}/cm^2$. An insulation layer 2, such as silicon dioxide SiO_2, is formed on the substrate surface. The pixel structure has a non-carrier storing, carrier collecting region 3 formed in the surface region of the semiconductor substrate 1, with a dopant of a second conductivity type which is opposite to the first conductivity type at a second concentration density. This carrier attracting region 3 is illustrated in Fig. 1 to be an n-implanted region, and it forms a photodiode junction with the p-type semiconductor substrate 1. The photodiode acts as a non-carrier storing, carrier generating region. The carrier collecting region 3 collects and/or attracts the carriers generated by incident radiation. For example, positive charges of an n- implant regions 3 attract photoelectrically generated electrons. The n- implant dopant density is so low (e.g. a concentration of 1 to 2 x $10^{16}/cm^2$) that it is in normal use always depleted, which means that no free charges are available, i.e. no storage of charge. The concentration can even be so low that it does not invert the background concentration of acceptors in the substrate. The carrier transport type in this region is lateral and diffusion limited. Charges are moved in the direction of lower potential from the p- to n regions of the diode junction. In the substrate 1 furthermore a doped or inverted region 4 of a second conductivity type is formed. This doped or inverted region 4 is illustrated in Fig. 1 to

be an n+ implant, with a concentration of a dopant which is higher than the concentration of dopant in the carrier collecting region 3. For example, the doped region 4 may be heavily doped, which means that there are so many donors that there are always free carriers available. A non-carrier storing, planar current flow, carrier transport region 5 is provided between the carrier collecting region 3 and the doped region 4. The doped region 4 is coupled to detection circuitry 6. The triangular "amplifier" symbol of the detection circuitry 6 represents any amplifier or readout structure that is can be used in pixels. A gate electrode 7 is formed on the insulation layer 2, and extends over the surface of the transport region 5.

When the substrate 1 is exposed to light, free carriers, e.g. electrons e^-, are generated in the substrate 1, where they may move freely. As the dopant concentration in the carrier collecting region 3 is so low that it is in normal use always depleted, an energy drop exists between the carrier collecting region 3 (n-implant) and the p substrate 1, so that the carrier collecting region 3 will attract electrons e^-. It does not, however, contain a neutral area, and can thus not store charge in such a neutral area nor is it intended to store charges in this region. If the gate electrode 7 is biased high, a conducting pathway (n-type inversion layer) is temporarily created in the transport region 5. The charges present in the neighbourhood of the carrier collecting region 3 can travel through the transport region 5 to the doped region 4, which forms a local energy minimum, i.e. a carrier storing region. Charges are moved through the transport region 5 by diffusion. At the doped region 4 there is a connection to the detection circuitry 6, such as a charge amplifier. The amplifier may be local to (active pixel) or remote from (passive pixel) the pixel structure.

As represented in dotted lines in Fig. 1, p well implants may be provided for confining the carrier collecting region 3.

The pixel structure described above with relation to Fig. 1 may be used to form a new structure, as represented in Fig. 2, which in fact places next to each other two or more of the pixel structures as described with relation to Fig. 1. This new structure may be used to divert the generated photocharge toward different collection bins in very short time spans. This feature is useful to switch on or off the photodetection as a function of time, which may be used for laser time domain reflectometry, to measure the time delay of a reflected laser light pulse. This short switching time would not be possible if charge were to stored at intermediate positions.

In a p-type substrate 1, for example, with an insulation layer 2 formed on the

substrate surface, an n- implant forms a non-carrier storing carrier collecting region 3. The n- implant has typically a very low dopant concentration, so as to deplete easily. Two n+ implants form a first and a second doped region 4, 4' at either side of the carrier collecting region 3. A first and a second planar transport region 5, 5' are respectively present between the carrier collecting region 3 and each of the doped regions 4, 4'. A first and a second gate electrode 7, 7' are formed on the insulation layer 2, each extending over the surface of one of the transport regions 5, 5'.

For using this pixel structure as a range pixel in laser time domain reflectometry, a short pulse of laser light is emitted towards and object, from where it is reflected to the range pixel represented in Fig. 2. The substrate 1 is exposed to light, and free electrons e^- are generated, which are attracted by the carrier collecting region 3. This carrier collecting region 3 does not serve to store charges, as it is so lowly doped that it is, in normal use, always depleted. The charge collected in the potential valley of carrier collecting region 3 is drained through any of the transport regions 5, 5' (by diffusion) and accumulated either to the left or to the right, depending on the voltage on the gate electrodes 7 and 7'.

The first gate electrode 7 is biased high for a certain amount of time T1, which temporarily creates a diffusion path (n-type inversion layer) in the first transport region 5. The second gate electrode 7' is biased low at the same time. The charges present in the neighbourhood of the carrier collecting region 3 can travel through the transport region 5 to the first doped region 4, where they are stored. After the time interval T1, the first gate electrode 7 is biased low, and the diffusion path in the first transport region 5 disappears. At the same time, the second gate electrode 7' is biased high for a certain amount of time T2. This temporarily creates a diffusion path (n-type inversion layer) in the second transport region 5'. The charges present in the neighbourhood of the carrier collecting region 3 can now travel through the transport region 5' to the second doped region 4', where they are stored. After different measurements, the charges on the first and the second doped regions 4, 4' are read out respectively by means of the detection circuitry 6 and 6'. The amount of charge collected in each of the doped regions 4, 4' can be used to determine a measure of the distance between the range pixel and the object reflecting the laser light.

The action of the range pixel is dependent upon transferring a quantitative amount of carriers from the carrier generating region to the region 4 so that the amount of this charge may be used in quantitative measurements. For the range pixel to function well, it is important that the carrier collecting region 3 cannot store

charge, otherwise charges stored in the carrier collecting region 3 during T1, might be transferred to the second doped region 4' during T2, thus being added to the charges generated during T2. Also charge which should have been transported in time T1 are stored in region 3 rather than being transported. Therefore, the carrier collecting region 3 is preferably very lowly doped.

As represented in dotted lines in Fig. 2, p well implants may be provided for as collecting region confining regions. They confine the carriers to the carrier collecting region 3.

An improvement on a pixel structure for use in laser time domain reflectometry is a structure identical to the one described in Fig. 2, except that there are more circuits comprising gate + doped region + detection circuitry that are connected to the carrier collecting region 3. Each of said circuits is able to accumulate the charge that is generated in the carrier collecting region 3 during a certain time slot, which time slot is defined by the time that the gates 7, 7', etc. are open. This allows carrying out measurements for bigger distances.

Furthermore, there may be an additional reset switch (not represented) connected to the carrier collecting region 3, which forms a diode with the substrate 1. The said additional reset switch can serve to drain the photocharge during the time that it is not accumulated by any of the said circuits.

It is also possible to have the structure of Fig. 1 with an additional reset switch (not represented) connected to the carrier collecting region 3.

Fig. 3 illustrates a further embodiment of a pixel structure of the present invention used for laser time domain reflectometry. It may be used in an active or passive pixel. It is a simplification of the pixel structure of Fig. 2. The simplification consists of a simplification in the processing, by the omission of the n- implant. If the n- implant is simply omitted, it would be expected that the danger exists that the photocharge generated in the bulk substrate 1 is not attracted/collected anymore at the surface, as it was the n- to substrate p- junction which had a built in electric field that drew and confined electrons to the surface. It has been found surprisingly that, if the n- implant is omitted, the electrons still are attracted and confined to the surface. This can be explained relying on two effects, either alone or in combination:

- Denuding at the surface. Boron (the most common p-type implant ion) easily diffuses to the SiO_2, so that the p-type Si-layer (substrate) close to the surface typically has a lower p concentration than the deeper layers. The depth of this "denuded" zone 10 is typically 100 nm. The difference in concentration between the p substrate 1 and the denuded zone 10 is a weak homojunction, and creates

a weak electric field that will draw free electrons e^- to the surface, from where they will further diffuse to the doped regions 4, 4' over the transport regions 5, 5'. Positive charge 11 in the covering silicon oxide 12. Silicon oxide as deposited or grown typically has a positive charge concentration of 1×10^{11} to 1×10^{12} positive ions per cm^3. This positive charge will induce an electric field near the interface between the substrate 1 and the covering oxide 12 that also attracts electrons.

The person skilled in the art would normally avoid using the interface between the substrate 1 and the covering oxide 12 as this layer is normally considered to be unreliable, i.e. having variable properties. It is this interface which can be used advantageously according to an embodiment of the present invention.

As represented in dotted lines in Fig. 3, p well implants may be provided for confining the carrier collecting region 3.

Fig. 4 is a schematic representation of a potential diagram which may be used to explain embodiments of the present invention, without being limited by theory. An electron is photo-generated in the substrate 1 and is collected in the collecting region 3 which acts in some ways like a gutter collecting rain off a roof. The collecting region 3 is unable to store any charge so that the collected electrons diffuse towards an area of lower potential, e.g. the region 4. Preferably, the collecting region is surrounded on appropriate sides with confining regions to prevent the collected electrons from diffusing in other unwanted directions. Hence, the potential diagram of the non-carrier storing collecting region and the non-carrier storing transfer pathway according to any of the embodiments of the present invention may be described as a potential saddle point. This means that the potential rises on both sides of a valley which sinks at at least one end to a lower level. The saddle collects the carriers without storing them. The carriers migrate or diffuse from the substrate where they have been photogenerated into the saddle region. They migrate or diffuse from the highest point of the bottom of the saddle to a lower point.

Normally in arrays of pixels, as used in an imaging device, pixels are square, but sometimes they may be longer in one direction, as represented in Fig. 5. Typically such an array can have photodiodes with a length L of 2000 µm and a width W of 7 µm. In a CCD technology, such a long photo receptor size is not a problem. Charges can be transferred from the storage gate to a floating diffusion structure with a relatively low capacitance (e.g. 5 fF) and be readout with much higher charge to voltage ratio. In a CMOS technology, it is a problem that such a

diode is physically long, has a long periphery, and has thus a large capacitance. The quoted size unavoidably has a capacitance of at least 50 to 100 fF in a typical 0.5μ CMOS technology, which means that it has a low sensitivity.

Fig. 6a and Fig. 6b illustrate a pixel structure in accordance with an embodiment of the present invention which can be used in an array of elongated pixels. The pixel structure may be used in an active or passive pixel. Fig. 6a illustrates a cross-section along a longitudinal axis of the elongate pixel, while Fig. 6b illustrates a transverse cross-section.

A p-type semiconductor substrate 1 is provided with an elongated non-carrier storing, carrier collecting region 3 in the longitudinal direction of the elongated pixel. This carrier collecting region 3 is formed by a depletable n- implant, and is thus a lowly doped region in which there are, in normal use, no free carriers. The carrier collecting region 3 forms a photodiode junction with the semiconductor substrate 1. Furthermore, a heavily doped region 4 is provided. A non-carrier storing, planar current flow, carrier transport region 5 is provided between the carrier collecting region 3 and the doped region 4. The doped region 4 is coupled to detection circuitry 6, which again may be any detection circuitry used in pixels. The pixel structure is preferably fabricated by MOS processing technology.

When the substrate 1 is exposed to light, free carriers, for example, electrons e^-, are generated in the substrate 1, where they may move freely. There is an energy drop between the carrier collecting region 3 and the p substrate. The carrier collecting region 3 attracts free electrons e^- towards the surface of the substrate 1. The collected electrons diffuse towards an energy minimum in the doped region 4, and accordingly are transported in the longitudinal direction of the pixel towards that region 4, where they are stored until they are read out by the detection circuitry 6. In the longitudinal direction, p wells 8 may optionally be provided near the carrier collecting region 3, as indicated by dotted lines in Fig. 6a, for confining the carrier collecting region 3.

In the transverse direction of the elongated pixel, p-wells 13 may, but need not, be provided at either side of the carrier collecting region 3 to further confine said region 3, as represented by dotted lines in Fig. 6b. Furthermore, P+ implants 15 may be provided between the field oxide 14 and the carrier collecting region 3 to avoid touching of the n- implant and the field oxide, as this can give rise to enhanced generation of dark current. Dark current is an offset error given by the signal charge that the pixel collects in the absence of light, divided by the integration

time. Dark current is temperature-sensitive and typically normalised by area (e.g. pA/cm^2)

The described embodiment provides an elongated diode with low effective capacitance. The large, elongated part of the photodiode is made such that it can collect (attract) charges, but not store them. Only a small part of the receptor is a real diode with highly doped n+ regions. The circuit that senses the diode node senses a small capacitance, which is nothing else than dQ/dV being small, or that a large voltage signal is generated by a small Q.

A further embodiment of a pixel structure according to the present invention is represented in Figs. 7a and 7b. Fig. 7a illustrates a cross-section along a longitudinal axis of the pixel, while Fig. 7b illustrates a transverse cross-section. The pixel structure may be used in an active or passive pixel. A p-type substrate 1 with a covering oxide 12 is provided. As in the device described in Fig. 3, a lowly doped implant for obtaining a non-carrier storing, carrier collecting region 3 in the substrate 1, is omitted. When the substrate 1 is exposed to light, free electrons e^- are generated in the substrate 1. These free electrons e^- are attracted by the carrier collecting region 3 and confined to the surface, relying on a boron denuded zone 10 at the surface creating a weak electric field in the p- to p homojunction and/or a positive space charge 11 present in the covering oxide 12.

In the longitudinal direction of the elongated pixel (Fig. 7a) and in the transverse direction of that pixel (Fig. 7b), p wells are provided at either side of the carrier collecting region 3 for confining the collecting volume, and to avoid that electrons are attracted by the field oxide 14 instead of by the covering oxide 12 on top of the active area (=desired carrier collecting area). If these p wells were not present, the electrons e^- would diffuse in all directions.

As represented by dotted lines in Fig. 7b, in the transverse direction of the elongated pixel, P+ implants may furthermore optionally be provided at either side of the carrier collecting region 3, between the carrier collecting region 3 and the field oxide 14, thus avoiding touching of carrier collection region 3 and the field oxide 14, as this, as already mentioned, can give rise to enhanced generation of dark current.

As the field oxide 14 is also an oxide, it is also positively charged, and the carrier collecting region 3 can be placed under the field oxide 14, as represented in Figs. 8a and 8b. Fig. 8a illustrates a cross-section along a longitudinal axis of a pixel according to an embodiment of the present invention, while Fig. 8b illustrates a transverse cross-section thereof.

A p-type substrate 1 covered with a field oxide 14 is provided. Again, a lowly

doped n- implant region 3 is omitted. Instead, when the substrate 1 is exposed to light, free electrons e^- are generated in the substrate 1, and attracted by the carrier collecting region 3 and confined to the surface, relying on a boron denuded zone at the surface creating a weak electric field in the p- to p homojunction and/or a positive space charge 11 present in the field oxide 14. In the longitudinal direction of the elongated pixel (Fig. 8a) and in the transverse direction of the elongated pixel (Fig. 8b), p wells 8, 13 may be provided at either side of the carrier collecting region 3 for confining the collecting volume and to avoid that the electrons e^- are attracted by the wrong places.

As represented by dotted lines in Fig. 8b, in the transverse direction of the elongated active pixel, P+ implants may optionally, but need not, be provided at either side of the field oxide 14, thus avoiding enhanced generation of dark current.

In Fig. 9a and Fig. 9b is illustrated a further embodiment of the present invention which uses a buried diode adjacent to a normal diode. Fig. 9a illustrates a cross-section along a longitudinal axis of the elongated pixel, while Fig. 9b illustrates a transverse cross-section thereof.

A p-type semiconductor substrate 1 is provided with an elongated non-carrier storing carrier collecting region 3 in the longitudinal direction of the elongated pixel. This carrier collecting region 3 is formed by a depleted n- implant, and is thus a very lowly doped region in which there are, in normal use, no free carriers. The carrier collecting region 3 forms a photodiode junction with the semiconductor substrate 1. It is buried by a P+ implant 9 on top of the carrier collecting region 3. Furthermore, a heavily doped region 4 is provided. A non-carrier storing, planar current flow, carrier transport region 5 is provided through the carrier collecting region 3 and the doped region 4. The doped region 4 is coupled to detection circuitry 6, which may be any detection circuitry used in pixels.

When the substrate 1 is exposed to light, free electrons e^- are generated in it, and they may move freely. There is an energy drop between the carrier collecting region 3 and the p substrate 1. The carrier collecting region 3 attracts free electrons e^-. The collected electrons e^- diffuse to an energy minimum in the doped region 4, and therefore are transported in the longitudinal direction of the elongated pixel towards that region 4, where they are stored until they are read out by the detection circuitry 6. In the longitudinal direction and the transverse direction of the elongated pixel, p wells 8, 13 may optionally be provided at either side of the carrier collecting region 3 to further confine said region 3, as indicated by dotted lines in Figs. 9a and 9b.

The P+ implant 9 on top of the carrier collecting region 3 avoids touching of the n- implant and the field oxide 14, which is advantageous as this touching can give rise to enhanced generation of dark current.

Fig. 10a and Fig. 10b illustrate a further embodiment of an elongated active or passive pixel of the present invention. Fig. 10a illustrates a cross-section along a longitudinal axis of the elongated pixel, while Fig. 10b illustrates a transverse cross-section.

A p-type substrate 1 is provided. When it is exposed to light, free electrons e^- are generated in the substrate 1. Above the substrate, a polysilicon gate electrode 7 is provided, the potential of which attracts the electrons e^- to the surface of the substrate 1. This potential should be high enough to attract but low enough not to capture or store the carriers. Under the polysilicon gate, a carrier collecting region 3 and a transport region 5, both being the same depletion layer, are created. The carrier collecting region 3 draws the electrons to the surface and the transport region 5 transports the electrons to a doped region 4.

In the longitudinal direction of the elongated pixel (Fig. 10a) and in the transverse direction of the elongated pixel (Fig. 10b), p-well implants 8, 13 may be provided at either side of the carrier collecting region 3 for confining the collecting volume and to avoid that the electrons e^- are attracted to the wrong places, e.g. by the field oxide 14 instead of the polysilicon gate electrode 7.

As represented by dotted lines in Fig. 10b, in the transverse direction of the elongated pixel, P+ implants may optionally be provided at either side of the carrier collecting region 3, thus avoiding electron collection by the active area that is not covered by the electrode 7, and also avoiding touching of the carrier collecting region 3 and the field oxide 14, as this can give rise to enhanced generation of dark current.

The features of all of the embodiments of the pixel structures described above may be manufactured in MOS technology. The structures of all these embodiments, but especially the structure of Fig. 10a, can also be used for making CCD's or CCD-like structures in CMOS technology (CCD – charge coupled device). The preferred embodiment of the structure of Fig. 10a used for making a CCD is represented in Fig. 11. The structure is as the one of Fig. 10a, except that the polysilicon gate 7 is replaced by a set of polysilicon gates 7', 7'', 7'''. By biasing each of the polysilicon gates 7', 7'', 7''' low or high, charges can be stored under the polysilicon gates or pushed away.

It is advantageous to make a CCD in a zone that is free of both n well and p

well implants. This results in the high fill factor effect as described in US patent application with the Serial No. 09/021,010, details of which are incorporated herein by reference.

The above active or passive pixels, but also other pixels known in the art, can be used in an array of pixels that is useful in an extended range of illumination conditions. Therefore, pixels of various sensitivities are mixed in the same array. At dark illumination levels, only the most sensitive ones will respond. At high illumination levels however, these sensitive pixels will saturate, and give thus no change in signal. At these illumination conditions, however, pixels with lower sensitivity will still give a useful response.

An embodiment of a design of an array of pixels with two types of sensitivities is symbolically represented in Fig. 12. According to an alternative embodiment (not represented), there are more than two types of pixels. Even a continuum of sensitivity ranges is possible. In the symbolic representation of Fig. 12, the large squares 20 represent sensitive pixels, and the small squares 21 represent less sensitive pixels. Pixels of the same type are organised on checkerboard patterns. In alternative embodiments, they may be organised also on lines, or on any pattern, even random. It is advantageous to have all pixels on the same line (or on the same output channel) with the same sensitivity, as otherwise signal steps will occur in the signal of a channel, possibly yielding problems with signal mixing.

Responses of individual pixels may be linear, but also non-linear responses make are included within the invention.

The effective size of the different pixel types may, but need not, be different. For example, if sensitive and less sensitive pixels are mixed, more area can be allotted to the sensitive pixels 20 than to the insensitive pixels 21.

The above structure is also applicable in cases where the signal of the pixels is not a function of the intensity, but of some other feature in the image, e.g. pixels may be designed to yield distance, colour, hue, speed, etc. The desired signal/response of pixels could be independent of the sensitivity, yet different types of pixels will be "active" in different ranges of illumination.

This design of an array of pixels can be used for a range camera with a high dynamic range. Note that resolution may be sacrificed due to part of the pixels not being active at any moment in time.

A passive pixel or an active pixel as represented symbolically in Fig. 13a or Fig. 13b, or in cross-section in Fig. 14, can be used to obtain a "synchronous shutter" or a "rolling curtain type of shutter". The active pixel represented in

Figs. 13a, 13b and 14 is a 4T (four transistor) pixel. It comprises a photosensitive element 24, a reset switch 25, a sample switch 26, and readout circuitry 27 comprising a readout switch 28 and a select switch 29 for choosing to where the result is to be output. Switches 25, 26, 28 and 29 are shown as transistors, preferably MOS-based transistors. An amplifier may be located at and connected to each pixel (active pixel) or the amplifier may be located remotely from each pixel (passive pixel). A synchronous shutter is a type of electronic shutter where all pixels in the imager are sensitive to light during exactly the same time span. All pixels collect charges at the same time; thereafter they are read out sequentially. This differs from a rolling curtain shutter, where the time span of light sensitivity depends on the pixel's position in the image.

Pixels are sensitive to light during an effective integration time. Integration time is the time that the sensor has to integrate photo-generated signal charge. The effective integration time of a pixel is defined more formally by the time between the reset of the photosensitive element 24 (the reset ends when the signal on the gate of the transistor of the reset switch 25 goes down) and the sampling of the signal of the photosensitive element (this sampling freezes the level when the signal on the gate of the transistor of the sample switch 26 goes down). After that, the information on the signal of the pixel is stored on the gate C of the transistor of the readout switch 28, and is ready for subsequent readout by means of the transistor of the select switch 29.

If reset and sample occur for all pixels at the same moment in time, a "synchronous shutter" is obtained. If reset and sample occur on a line-by-line basis, at the same rate as the normal line readout speed, a "rolling curtain type" of shutter is obtained. A disadvantage of known synchronous shutter pixels is that it is not possible to readout and integrate at the same time.

According to Figs. 13a, 13b and 14, the pixel has as photosensitive element 24 a buried diode. This buried diode is formed by an n implant 30, which forms a diode with the p substrate 32, with on top of it a P+ implant 31 burying the diode. The buried diode may, but does not have to be, a depletable diode. The main goal of the buried diode is not full charge transfer, but the isolation of the pn junction from the surface of the pixel during the integration time. As during the integration time (collection of free electrons e^-), both reset and sample are off, the junction does not touch the $Si\text{-}SiO_2$ interface, and suffers less from dark current.

In the embodiment described in Fig. 14, the p-well 37 is optional, as well as the P+ burying layer 31 of the diode 24. If the p-well 37 is taken out, the N+ implant

36 is more light sensitive. The pixel will work but not as well as with the N+ implant 36. Another pixel which is suitable for use in this embodiment of the present invention is shown in Fig. 4 of US 6,011,251 whose description is incorporated herein by reference.

In use of the synchronous shutter pixel of fig. 14, light falls in on the substrate 32 and free electrons e^- are formed. They are attracted towards the n implant region 30 due to the weak electric field of the pn junction.

For controlling the switches 25, 26, 28, 29 a timing circuit is provided which may be a conventional timing circuit modified to provide the additional novel features of this embodiment of the present invention. In Fig. 15a a time diagram is represented which is carried out by the timing circuit. The timing circuit shows pulses occurring for all pixels and lines in parallel. It shows that at a time T0 both reset and sample signals go high, which means that the reset gate electrode 33 of the reset transistor 25 and the sample gate electrode 34 of the sample transistor 26 are biased high. Inversion layers are created under both gate electrodes 33, 34, such that all charges present in the n implant 30, in the N+ implant 36 and on the gate of the readout transistor 28 are evacuated towards the N+ implant 35. At T1, the signal on the sample gate 34 of the sample transistor 26 goes down, which means that the inversion layer under sample gate 34 disappears, and that charges no longer flow between the diode 24 and the N+ region 36. At that moment, the signal on the reset gate 33 of the reset transistor 25 stays high. At T2, the signal on the reset gate 33 of the reset transistor 25 goes down, which means that the inversion layer under reset gate 33 disappears, and that charges no longer flow between the diode 24 and the N+ implant 35. The N+ region 36 and the diode 24 are now reset. During a time period (indicated in Fig. 15a as the time span between T2 and T3, the integration time) light falling in on the substrate 32 generates free electrons e^-, which are collected by the diode 24. At T3, the signal on the sample gate 34 of the sample transistor 26 goes high, thus creating an inversion layer under this electrode. Charge collected by diode 24 is transferred to N+ implant 36 where it is stored for readout. Hence, N+ implant 36 functions as a charge storing element or memory element. The charge storing element may be implemented as an analog memory element such as a capacitor or a parasitic capacitor. Reference is made to Fig. 4 and the related description of US 6,011,251. At T4, the signal on the sample gate 34 of the sample transistor 26 goes low. Therefore, the inversion layer under sample gate 34 disappears, and charges are no longer transferred towards N+ implant 36.

The reset and sample pulses as represented in Fig. 15 occur synchronously (i.e. all at the same time) for all pixels to determine the effective integration time.

A time diagram for reading out the pixels is represented in Fig. 15b. At time T5, the signal on the gate of the select transistor 29 goes high, thus selecting a line to be read out. At the same moment, the signal on the reset gate 33 of the reset transistor 25 goes high, thus evacuating free charges, further collected by the diode 24 during readout of the pixel, towards N+ implant 35. At time T6, the signal on the reset gate 33 of reset transistor 25 goes down again, and charges of diode 25 are no longer evacuated towards N+ implant 35. Shortly after, at time T7, the signal on the sample gate 34 of the sample transistor 26 goes high. The pixel is read out (signal level). At T8, the signal on the reset gate 33 of the reset transistor 25 goes high again. The signal on the sample gate 34 of the sample transistor 26 still being high, N+ implant 36 and diode 24 are reset. At T9 the signal on the reset gate 33 of the reset transistor 25 goes down again. A reset level of the pixel is read out. Due to this, on-chip offset correction can be performed (sometimes called double sampling or correlated double sampling). At T10, both the signals on the sample gate 34 of the sample transistor 26 and on the gate of the select transistor 29 go down. Readout of the following line of pixels can start.

During readout, the reset and sample pulses are applied on a line by line basis in order to allow readout of signal and reset levels.

The time diagram of Fig. 15a occurs once per frame, while the time diagram of Fig. 15b occurs once for each line.

The advantage of the current synchronous shutter pixel is that the reset gate is now on another place than the sample gate, so that it is possible to reset while the pixel is being read out.

The time diagrams of Figs.15a and 15b can be combined in the concept of range pixel described in Fig.2 to make a range pixel in which a pixel may be read-out simultaneously with all other pixels. As a range pixel has two carrier storing regions, the same carrier storing regions of the range pixels are read-out at the same time.

While the invention has been shown and described with reference to preferred embodiments, it will be understood by those skilled in the art that various changes or modifications in form and detail, such as configurations or materials, may be made without departing from the scope and spirit of this invention.